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Cotues et al.

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[54] **STEPPED ELECTRONIC DEVICE PACKAGE**

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[51] Int. Cl.[5] H05K 7/00; H01L 23/02
[52] U.S. Cl. 361/744; 361/729; 257/686; 437/209
[58] Field of Search 29/832, 832, 836, 840; 174/253, 260, 261; 228; 228/179, 180.2; 257/686, 79, 80; 361/393, 396, 396, 400, 403, 404, 405, 406, 412, 413; 439/62, 65, 66, 68, 71, 66, 91, 493

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[57] ABSTRACT

An electronic device packaging structure is described wherein an electronic device is electrically connected to a substrate wherein the electronic device subtends a non-normal angle with respect to the substrate. In a more specific embodiment, a plurality of electronic devices are stacked at offset with respect to each other to expose contact locations on the surface of each electronic device as an edge of each electronic device to form a stepped surface exposing a plurality of electronic device contact locations. This surface is disposed against a substrate having a plurality of contact locations thereon. The electronic device contact locations can be electrically interconnected to the substrate contact locations by solder mounds or alternatively by a cylindrical shaped elastomeric body having metallization bands with a spacing corresponding to the electronic device contact locations. The elastomeric body is pressed between the edge of the stacked electronic devices having the contact locations thereon and substrate surface to form electrical interconnections between electronic device contact locations and substrate contact locations through the electrically conducting bands. The stacked electronic devices can be thermally connected to a heat dissipation member. The stacked electronic devices can have a stepped surface embodying an enhanced area for transfer of heat from the electronic device stack to the heat dissipation member.

9 Claims, 6 Drawing Sheets

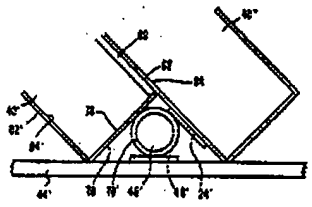


FIG. 4

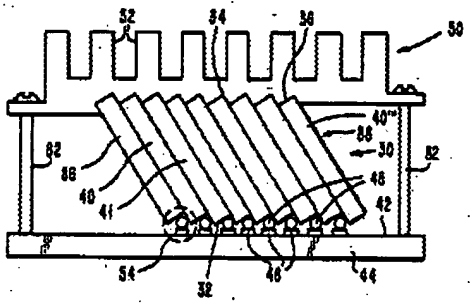
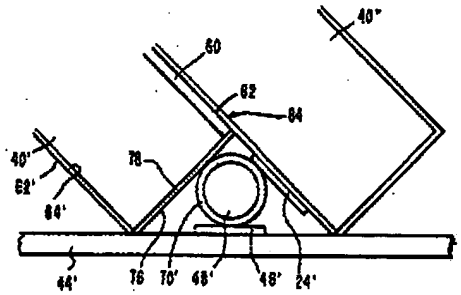


FIG. 5



nular aspect of the present invention, a onic devices are disposed in a stack electronic device has an edge having t location thereon and wherein elec- arranged to expose the contact loca- edge by forming a stepped surface side of the electronic device stack.

e particular aspect of the present in- onic device stack is disposed against a a plurality of contact locations ng at least one substrate contact loca- onnected to at least one contact loca-

particular aspect of the present inven- al interconnection between the chip and the substrate contact location ical conductor bearing elastomeric osed between the chip contact loca- rate contact location.

e particular aspect of the present in- onic device stack has at least one ace for thermal connection to a heat

IPTION OF THE DRAWINGS

matic representation of one chip hav- ns thereon along an edge electrically substrate having contact locations the chip subtends a non-orthogonal to the substrate.

plurality of chips stacked in a non- ement.

n elongated cylinder having electri- bands thereon which is used as the nector between the chip contact loca- rate contact locations in the embodi- IGS. 4 and 5.

e chip stack of FIG. 2 with the struc- the electrical interconnection means isposed in connection with the chip

rged view of the electrical intercon- FIG. 4.

n-orthogonal stacking of chips along endicular directions.

matically shows an apparatus and ting the stacked structure described

a stacked structure electrically con- trate by an interconnection means ed conductors in an elastomer.

another embodiment of the stepped esent invention with contact location y connected to substrate contact loca- a.

D DESCRIPTION OF THE RRED EMBODIMENT

view of an embodiment of the present te 2 has at least one contact location 4 ic device 6 has at least one contact or surface 8 along an edge 10. Elec- as an opposite surface 7. Electronic an angle 12 with respect to substrate non-orthogonal angle, that is not 90 c device 6 contact location 8 is elec- to substrate contact location 4 by nection means 13 which can be metal- lized elastomeric body as described herein below, and which can also be a solder interconnection; wireboard array, patterned conductive epoxy; liquid metal; spring loaded or spring contacts; e.g., fuzz buttons or any other electrical interconnection means.

FIG. 2 shows a plurality of electronic devices 14, 16, 18 and 20, which are stacked one on top of each other. Electronic devices 16, 18 and 20 are disposed in intimate contact with respect to each other. Electronic device 14 is shown spaced away from electronic device 16 for the purpose of showing how the electronic devices are stacked. FIG. 2 shows four electronic devices in a stack. The structure of FIG. 2 is not limited to four, there can be any number of electronic devices in a stack. Each electronic device can be any type of an electronic device such as a dielectric material having electrically conducting lines therein, for example a printed circuit board and a metallized ceramic. Alternatively, electronic devices of FIG. 2 can be semiconductor chips, for example, silicon chips and gallium arsenide chips. Each electronic device is stacked onto an adjacent device with an edge of each device set back by a distance 22 from the adjacent device. The setback is preferably the same between each device. Each device has at least one contact location 24, preferably a plurality of contact locations along an edge region 26. The setback 22 results in the contact locations 24 being exposed for each device. In the preferred embodiment, the top device in the stack 14 is preferably a dummy device, that is having no electrical function but having a structural function but this is not necessary. If the setback 22 of each device is equal, the structure has a stack angle 28. The resultant stacked chip structure 30 has a stepped or staircased edge 32 with exposed electronic device contact locations and if the electronic devices are of the same dimension, there is a corresponding stepped or staircased surface 34 which can have additional chip contact locations or can be without device contact locations. The structure of FIG. 2 shows each electronic device stepped back from an adjacent electronic device along the same direction 36. Between each adjacent electronic device such as 16 and 18 there is preferably an adhesive, such as an epoxy cement to keep each electronic device of the stack 30 physically adhering together. An adhesive layer is not shown in FIG. 2. Alternatively, the electronic devices of the stack 30 can be mechanically held together by a clamp. There may also be spacers placed between the devices.

FIG. 4 shows an electronic device stack 30 having nine electronic devices 40 in the stack. Electronic device stack 30 edge 32 having the exposed electronic device contact locations is disposed adjacent surface 42 of substrate 44. Surface 42 of substrate 44 has a plurality of contact locations 46 thereon. Contact locations 46 are electrically interconnected to contact locations 24 of electronic devices 40 by means 48 which can be a plurality of solder mounds disposed between electronic device contact locations 24 and a corresponding substrate contact location 46. Where solder mounds are used the controlled-collapse-chip-connection methods described in U.S. Pat. Nos. 3,401,126 and 3,429,040 to Miller, the teachings of which are incorporated herein by reference. Stepped edge 34 of electronic device stack 30 which is opposite to stepped edge 32 is disposed in to a stepped groove 36 in the surface of heat sink 38. The stepped surface 34 of electronic device stack 30 provides an enlarged surface area than would be provided if each electronic device were stacked orthogonally on

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electronic device is located on the corresponding step 130 fixture 140 and not the previous electronic device.

(16) Step 5--Go to step two to load the next electronic device.

(17) FIG. 8 is a diagrammatical cross section, similar to that of FIG. 5, showing an alternate means for electrically interconnecting the electronic device contact pads 224 in electronic devices 240. Wires 250 are bonded at one end 252 thereof to the electronic device contact pads 224. The wires can be, for example, of Au, Al and Cu, for example of 0.001 to 0.003 inch diameter. The joint between ends 252 and contact locations 224 can be a wire bond. The bonds can be a flattened ball bonds or wedge bonds both of which are commonly practiced in the art. The wires are bent at an angle to the electronic devices surface 254 by jogging the bonder platform that the part rests upon after to bond is made. The end 256 of wire 250 is severed at a predetermined position. The ends 256 may be bent, laser-formed into ball shapes or left as straight wires. End positions may be manipulated to assure a given grid geometry for contact to substrate contact locations 246. The array is then encapsulated in an elastomeric, e.g. silicone, material leaving the ends of the leads free. There are two preferred methods for encapsulation of the leads. The first is to fixture the array so that the balls form a plane at the top of the part, and then to introduce a controlled volume of liquid encapsulant into the area of the leads. The spaces between the leads fills by capillary attraction and stops at the base of the balls. The liquid is then cured at elevated temperature. The second method is to first encase the lead ends in a water soluble solid, i.e., sugar, by dipping into the liquid form and then drying. Liquid elastomer is then forced under pressure into the space to be filled and cured. The water soluble cap is then dissolved away exposing the ends of the leads. The assembly may be pressed to the substrate or solder bonded as described above to the substrate contact locations 246 on substrate 244.

(18) FIG. 9 shows another embodiment of the stepped stack of chips shown in FIG. 2. The stack is disposed on a substrate 260 having a plurality of

FIG. 1

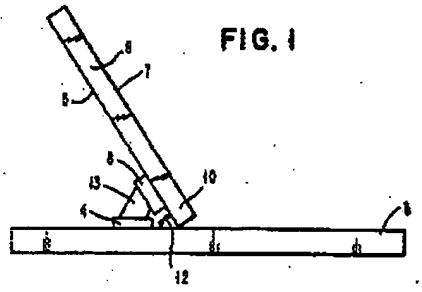


FIG. 2

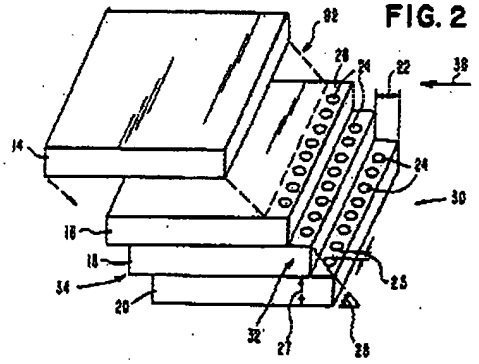
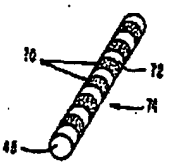


FIG. 3



In a more particular aspect of the present invention, a plurality of electronic devices are disposed in a stack and wherein each electronic device has an edge having at least one contact location thereon and wherein electronic devices are arranged to expose the contact location on each chip edge by forming a stepped surface along at least one side of the electronic device stack.

In another more particular aspect of the present invention, the electronic device stack is disposed against a substrate having a plurality of contact locations thereon, there being at least one substrate contact location electrically connected to at least one contact location.

Another more particular aspect of the present invention is the electrical interconnection between the chip contact location and the substrate contact location through an electrical conductor bearing elastomeric body which is disposed between the chip contact location and the substrate contact location.

In another more particular aspect of the present invention, the electronic device stack has at least one other stepped surface for thermal connection to a heat dissipation means.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic representation of one chip having contact locations thereon along an edge electrically connected to a substrate having contact locations thereon wherein the chip subtends a non-orthogonal angle with respect to the substrate.

FIG. 2 shows a plurality of chips stacked in a non-orthogonal arrangement.

FIG. 3 shows an elongated cylinder having electrically conducting bands thereon which is used as the electrical interconnector between the chip contact locations and the substrate contact locations in the embodiments shown in FIGS. 4 and 5.

FIG. 4 shows the chip stack of FIG. 2 with the structure of FIG. 3 as the electrical interconnection means and a heat sink disposed in connection with the chip stack.

FIG. 5 is an enlarged view of the electrical interconnection means of FIG. 4.

FIG. 6 shows non-orthogonal stacking of chips along two mutually perpendicular directions.

FIG. 7 diagrammatically shows an apparatus and method for fabricating the stacked structure described herein.

FIG. 8 shows a stacked structure electrically connected to a substrate by an interconnection means formed from formed conductors in an elastomer.

FIG. 9 shows another embodiment of the stepped structure of the present invention with contact location thereon electrically connected to substrate contact location by wire bonds.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 is a side view of an embodiment of the present invention. Substrate 2 has at least one contact location 4 thereon. Electronic device 6 has at least one contact location 8 on major surface 5 along an edge 10. Electronic device 6 has an opposite surface 7. Electronic device 6 subtends an angle 12 with respect to substrate 2. Angle 12 is a non-orthogonal angle, that is not 90 degrees. Electronic device 6 contact location 8 is electrically connected to substrate contact location 4 by electrical interconnection means 13 which can be metallized elastomeric body as which can also be a solder array, patterned conductiv loaded or spring contact other electrical interconne

FIG. 2 shows a plurality 18 and 20, which are stack Electronic devices 16, 18 a contact with respect to eac is shown spaced away fro purpose of showing how stacked. FIG. 2 shows thur The structure of FIG. 2 is be any number of electro electronic device can be a vice such as a dielectric conducting lines therein, board and a metallized c tronic devices of FIG. 2 for example, silicon chips Each electronic device is vice with an edge of each 22 from the adjacent devi the same between each de one contact location 24, contact locations along an 22 results in the contact lo each device. In the prefer vice in the stack 14 is prefe is having no electrical fun function but this is not ne each device is equal, the st The resultant stacked chip staircased edge 32 with contact locations and if the same dimension, there is staircased surface 34 whic contact locations or can be tions. The structure of FI device stepped back from along the same direction electronic device such as an adhesive, such as an electronic device of the together. An adhesive lay Alternatively, the electroni be mechanically held toge also be spacers placed bet

FIG. 4 shows an electr nine electronic devices 40 vice stack 30 edge 32 ha device contact locations is of substrate 44. Surface 42 of contact locations 46 ther electrically interconnected electronic devices 40 by m rality of solder mounds device contact locations 2 strate contact location 46 used the controlled-collap described in U.S. Pat. Nos Miller, the teachings of wh by reference. Stepped edge 30 which is opposite to step a stepped groove 36 in the stepped surface 34 of elec vides an enlarged surface If each electronic device w